5 Evaluation Boards

Here we discuss just a few of the many development boards which are widely available for the 8051 family of micro-controllers. These evaluation boards can be used to develop and test the program on the actual hardware and arte especially useful for students whilst gaining experience on the micro-controller. Actual add-on hardware (such as LCD displays, servo motors, LEDs, keyboards) can also be connected to these boards in order to implement the required project. We discuss and explain the main features of the Flite-32 board from Flite Electronics International Limited (http://www.flite.co.uk) using an 8032 micro-controller, the NMIY-0032 8051 board from New Micros, Inc. (http://www.newmicros.com) using an 8051 and the C8051F020TB from Silicon Labs (http://www.silabs.com) using the very high performance C8051F020 micro-controller. These are all available at the University of Malta Communications and Computer Engineering department laboratories for student use.

Naturally, if you are using another kind of board, you might wish to skip this chapter completely or just skim through it perhaps you might pick some new idea.

5.1 FLITE-32 Development Board

The FLITE-32 development board is available from Flite Electronics International Limited (see http://www.flite.co.uk/flite-flt-32-803251-training-system.htm), is used extensively in our course program to train the students on the 8051-family of microcontrollers. It uses the 8032 device, thus having available three timers and 256 bytes of internal RAM. Co effectively mplete schematics and manuals are available from this site.

The board also has some additional peripherals, which further enhance its capabilities. Namely it has:

- 32KB monitor EPROM program
- 8KB (which we have expanded to 32KB) external memory
- 8255 Peripheral Interface Adaptor IC providing an additional 24 I/O lines (3 I/O ports having 8-bits each)
- 26C91 Universal Asynchronous Receiver/Transmitter (UART) providing an additional serial port, running at a maximum of 38400 baud, using socket P2

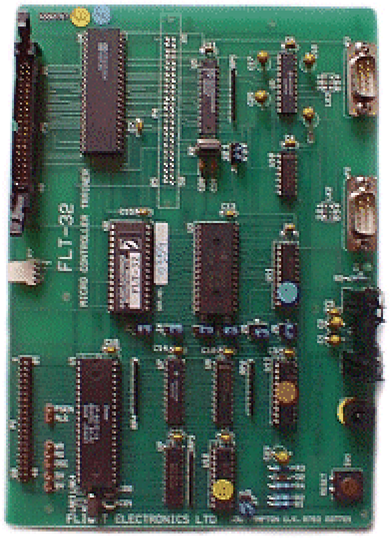

Figure 5-1 Flite-32 Board

5.1.1 FLITE-32 General Setup

Microprocessor: Intel 8032

Internal RAM: 256 bytes

External RAM: either 8KB using the 6264 SRAM IC.
(address 8000H to 9FFFH, with J2/J3 having links 2-3)
or 32KB using the 62256 SRAM IC.
(address 8000H to FDFFH, with J2/J3 links 1-2)

User area for code and data starts from 8100H

Reserved Areas: The monitor program residing in the 32KB EPROM, having Address range 0000 to 7FFFH, also uses some memory in the internal RAM and in the external RAM. In particular if some printing routines from the monitor are being used, internal RAM locations 20H and 21H should be avoided together with external RAM area 8000H to 80FFH.

5.1.2 Peripherals:

The lists below describe the address mapping and register names given to the peripherals found on the board.

8255 Input-Output IC:

Port A – FF40H

Port B – FF41H

Port C – FF42H

Control – FF43H

2691 External UART (P2):

```
UART_2691_BASE   EQU   0FFF8H              ; UART BASE ADDRESS, on Flite-32
UART_MR1         EQU   UART_2691_BASE      ; MR1 – Mode Register 1
UART_MR2         EQU   UART_2691_BASE      ; MR2 – Mode Register 2
UART_SR          EQU   UART_2691_BASE + 1; READ SR – Channel Status Register
UART_CSR         EQU   UART_2691_BASE + 1; WRITE CSR – Clock Select Register
UART_CR          EQU   UART_2691_BASE + 2; WRITE CR – Command Register
UART_RHR         EQU   UART_2691_BASE + 3; READ RHR – Rx Holding Reg
```

```
UART_THR        EQU   UART_2691_BASE + 3; WRITE THR – Tx Holding Reg
UART_ACR        EQU   UART_2691_BASE + 4; WRITE ACR – Auxiliary Control
UART_ISR        EQU   UART_2691_BASE + 5; READ ISR – Interrupt Status Register
UART_IMR        EQU   UART_2691_BASE + 5; WRITE IMR – Interrupt Mask Reg
UART_CTU        EQU   UART_2691_BASE + 6
; READ/WRITE CTU – Counter Timer Upper Register
UART_CTL        EQU   UART_2691_BASE + 7
; READ/WRITE CTL – Counter Timer Lower Register
RX              EQU   0FFE8H              ; READ RX DATA input (socket P2).
                                  ; This is used if required to auto-determine the baud rate
```

The 2691 can also be used under interrupt control, by connecting the link J8 to External 0 Interrupt (link 5-6), or External 1 Interrupt (link 5-4).

The main memory map of the board is shown in Table 5-1.

Internal RAM	External EPROM or RAM	Remarks
Not Available	FFFFH	UART
	FE40H	8255
	FE00H	Peripherals
	FDFFH If 32KB External RAM (Code and Data) A000H	User Area
	9FFFH 8KB External RAM (Code and Data) 8100H	User Area
	80FFH to 8000H	Reserved For monitor Use
FFH Internal On-chip Memory 00H	7FFFH External EPROM (Monitor Code Area) 0000H	Monitor Program

Table 5-1 FLT-32 Memory map

Additional RAM can be added by replacing the default RAM chip. Even the EPROM can be replaced with a smaller or larger capacity EPROM. In every case, some jumper links would have to be re-arranged to get the correct address coverage.

The Interrupt Vector Table, which normally resides in the low ROM area, (0000H to 0030H), is re-mapped on start-up and points to the external RAM area starting at 8000H. For example, in the monitor EPROM, at address location 0003H, which is the normal EXT0 interrupt vector address, there is written the instruction LJMP 8000H (jump to address 8000H).

Interrupt Number	0	1	2	3	4	5
Interrupt Name	External 0	Timer 0	External 1	Timer 1	Serial	Timer 2
Standard Vector Address	0003H	000BH	0013H	001BH	0023H	002BH
FLT-32 Vector Address (Monitor Version V0)	8000H	N/A	8010H	8018H	8020H	8028H
FLT-32 Vector Address (Monitor Version 3)	8000H	* 8008H	8010H	8018H	8020H	8028H
Flags Causing Interrupt	IE0	IT0	IE1	TF1	RI & TI	TF2 & EXF2
Interrupt Enable bit (+ EA)	EX0	ET0	EX1	ET1	ES	ET2
Interrupt Priority bit	PX0	PT0	PX1	PT1	PS	PT2
Falling Edge Triggering	IT0		IT1			

Table 5-2 FLT-32 Interrupt Vector Table

* This 8008H address is only available if using version 3 monitor EPROM which we modified. The modification in the EPROM involved over-writing locations starting at 0008H with a JMP 8008H instruction, thus replacing the original jump to the Single Step command which existed in the standard monitor program. Otherwise, it would not be available since this interrupt is normally used by the default EPROM monitor for the SINGLE STEP command.

Note:

Link J8 can be used to divert signals to EXT0 or EXT1 interrupt pins of the CPU as described here:

External Interrupt pin 5 on the optional P4 connector can be connected to EXT0 (link 2-3) or to EXT1 (link 1-2)

Also interrupts from the external 2691 UART can also be diverted to EXT0 (link 5-6) or to EXT1 (link 5-4)

Timers:

Timer 0 is used by the monitor Version 0 program (under interrupt control) whenever Single Step or Trace is being performed. Hence it is available to the user (not using interrupts since the vector is not available in RAM) providing no tracing is being done. Moreover, if the program is intended for stand-alone EPROM use (that is we eventually will replace the monitor EPROM with another EPROM which we will write ourselves containing just our application program), then even the interrupt can be used (using Timer 0 vector address 000BH). Otherwise, the interrupts connected with Timer 0 can only be used with the modified version 3 of the monitor program, which removes the Single Step function.

Timer 1 is used (not under interrupt control) as the baud rate generator whenever socket P3 (the 8032 internal UART) is being used by the monitor program, usually to output characters to a printer or to a terminal. Hence if the monitor routines for printing using socket P3 are not being used, then Timer 1 can be used in any mode as we deem fit.

Serial Printer:

Socket P3 (serial printer) is selected by pressing

W (set baud rate),

WO (enable printer) and

WX (disable printer),

when in the monitor prompt.

5.1.3 Some Important FLITE-32 Monitor Routines:

Use LCALL <address> to use these routines which are already coded in the monitor program. CALLed from the user program, they will RETurn on completion.

- 0090H Convert character in the ACC to upper case.
- 0093H Send the character in the ACC to external UART (socket P2).
- 0096H Get character from external UART (socket P2) to the ACC.
- 0099H Send Carriage Return and Line Feed to external UART (socket P2).
- 009CH Send to UART message pointed to by DPTR, terminated by 00H.
- 009FH Restart board without initialising.
- 00A2H As above but with sign-on message.
- 00A5H Send to UART the Hex word in found in registers AB as ASCII characters.
- 00A8H Convert the ASCII value in ACC to Hex.

It should be noted here that the monitor program makes use of the internal RAM memory from 00H to 5FH. In fact, the monitor program intialises the stack pointer SP to 5FH, thus having the actual stack starting at 60H. Use of the internal RAM area 00 to 7FH should be avoided if one intends to make use of the functions/commands of the monitor program. For the PaulOS RTOS, all monitor commands and functions are ignored, and all the 256 bytes of the internal RAM area, from 00H to FFH are used extensively by the RTOS and any application program which is running.

5.2 Typical Settings for KEIL uV2

USE the following settings in Options for Target 1

Memory Model:	LARGE: VARIABLES IN XDATA
Code Model:	LARGE: 64K Program

	START	SIZE	(If using 32KB RAM)
CODE:	0X8100	0X5D00	
RAM:	0XDE00	0X2000	

Interrupt Vector address at 0x7FFD (click on C51 tab)

	START	SIZE	(If using 8KB RAM)
CODE:	0X8100	0X1B00	
RAM:	0X9C00	0X0400	

Interrupt Vector address at 0x7FFD (click on C51 tab)

	START	SIZE	(If using 32KB EPROM)
CODE:	0X0000	0X8000	
RAM:	0X8000	0X7E00	

Interrupt Vector address at 0x0000 (click on C51 tab)

5.3 The NMIY-0031 Board

This is another low-cost 8051 evaluation board, available from New Micros Inc. (see http://www.newmicros.com/cgi-bin/store/order.cgi?form=prod_detail&part=NMIY-0031). Complete schematics and user manual are available from this site.

5.3.1 NMIY General Data

NMIY uses an 8051 micro-controller having two timers (T0 and T1), one UART (equivalent to the P3 socket found on the FLITE-32 board) and only 128 bytes internal RAM.

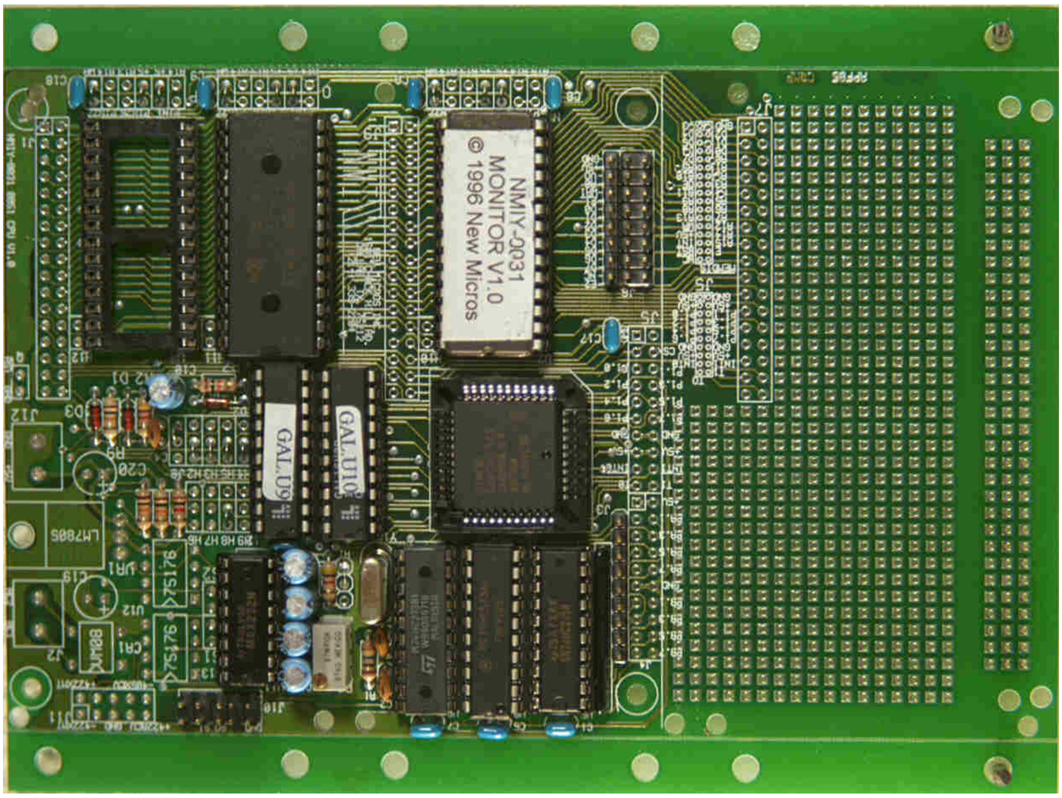

Figure 5-2 NMIY-0031 Board

T1 can be used for the serial port. The serial interrupt is not available when using the monitor EPROM.

Initially, whilst developing and loading the hex file onto the board, use only a serial baud-rate of 9600 baud (8-N-1-N), 2 ms/character and 5 ms/line delays in the terminal software (such as TERATERM) settings. The baud rate can then be changed to any standard value in the user's source file program, depending on the application requirements.

Use CAPITAL letters to talk to the monitor program:

H – Help
L – Load
X – Execute

As standard, the board has only 8KB of monitor code and 8KB of RAM to use for code and data. Additional RAM (for decimal/hex sizes see Table 5-3 where the hex size is shown using the 0x prefix notation instead of the H suffix notation) can be plugged in, up to 64Kbytes (say two 32KB RAM ICs in sockets U3 and U4). See link settings Table 5-4.

We may start program code from 8100H (same as in FLITE-32), so we may adjust the ORG position in the STARTUP.A51 file accordingly.

Also, in the STARTUP.A51 file, the IDATALEN has to be modified to 80H (128 bytes).

The Interrupt Vector Base address should be adjusted to 8000H (not 7FFDH as for the FLITE-32). This is because the interrupt vectors use slightly different mapping addresses than on the FLITE-32 board.

RAM SIZE KBYTES	RAM SIZE BYTES (DECIMAL)	RAM SIZE BYTES (HEX)
0.5	512	0x0200
1	1024	0x0400
2	2048	0x0800
3	3072	0x0C00
4	4096	0x1000
5	5120	0x1400
6	6144	0x1800
7	7166	0x1C00
8	8192	0x2000
9	9216	0x2400
10	10240	0x2800
11	11264	0x2C00
12	12288	0x3000
13	13312	0x3400
14	14336	0x3800
15	15360	0x3C00
16	16384	0x4000
17	17408	0x4400
18	18432	0x4800
19	19456	0x4C00
20	20480	0x5000
30	30720	0x7800
32	32768	0x8000

Table 5-3 RAM Size Dec-Hex Conversion

5.3.2 MEMORY MAPPING:

Addresses above 0XFC00 (or FC00H) are reserved.
In fact address 0xFFFC refers to the additional external IC input/output latched port.
This is available from the J4 socket.
You may use for example, in your C program:

```
#define MyPort          XBYTE [0XFFFC]
// define MyPort address (FFFCH) as the input/output port
// PB0 to PB7 will be the output bits
// PA0 to PA7 will be the input bits
unsigned char dataout, datain;

MyPort = dataout;       /* send data stored in variable dataout, to the output port (PB0-PB7) */
datain = MyPort;        /* read data from MyPort (PA0-PA7) to the datain variable */
```

Socket	**U2 (EPROM)**			**U3 (RAM)**		**U4 (RAM)**
	H3 (1-2) Code only	H3 (2-3) Code + Data	H4 32K or 64K	H2 (1-2) Code + Data	H2 (2-3) Data only	Data only
2764 8KB	N = 0011001 0x0000 – 0x1FFF		(1-2)	O = 011001 0x8000 – 0x9FFF		P = 011001 0x0000 - 0x1FFF
27128 16KB	N = 0010101 0x0000 – 0x3FFF		(1-2)	O = 010101 0x8000 – 0xBFFF		P = 010101 0x0000 – 0x3FFF
27256 32KB	N = 0010110 0x0000 – 0x7FFF		(1-2)	O = 100101 0x8000 – 0xFC00		P = 100101 0x0000 – 0x7FFF
27512 64K	N = 1000110 0x0000 – 0xFFFF		(2-3)	Not available		Not available

Table 5-4 External Memory (Link Settings)

Normally, whilst developing the program:

- U2 is set to code only (containing the monitor program)
- U3 is set to code + data
- U4 (if available) is set to data only (cannot set it in any other mode)

We must make sure to set the memory map in the Target Options to reflect our particular memory setup.

5.3.3 Input-Output connections

J4 is the latched input – output port (address 0xFFFC)
PA pins are the INPUT pins, and PB pins are the OUTPUT pins.
Pin 1 is in the direction of U1 and closest to U2.
Make sure that we have the correct pin orientation!

Pin No:	Signal	Pin No:	Signal
1	+5 V	2	+5 V
3	PA^0	4	PA^1
5	PA^2	6	PA^3
7	PA^4	8	PA^5
9	PA^6	10	PA^7
11	GND	12	GND
13	PB^0	14	PB^1
15	PB^2	16	PB^3
17	PB^4	18	PB^5
19	PB^6	20	PB^7

Table 5-5 NMIY J4 Pinouts

J5 is the 8051 port 1, external timer inputs and external interrupts.

Pin 1 is in the direction of U1 and closest to U2.

Make sure that we have the correct pin orientation!

Pin No:	Signal		Pin No:	Signal
1	GND		2	GND
3	RST		4	CSX
5	P1^0		6	P1^1
7	P1^2		8	P1^3
9	P1^4		10	P1^5
11	P1^6		12	P1^7
13	GND		14	GND
15	+5 V		16	+5 V
17	INT 0		18	INT 1
19	T0		20	T1

Table 5-6 NMIY J5 Pinouts

J6 is the LCD connector. P1 is located in the row nearest to U2 and closest to the board edge. Address 0xFFF8 is used to send COMMANDS and address 0xFFF9 is used for sending DATA to the LCD.

Pin No:	Signal		Pin No:	Signal		Pin No:	Signal
1	GND		2	+5 V		3	GND
4	CONTRAST		5	A0		6	CONTRAST
7	WR1		8	E1		9	WR1
10	D0		11	D1		12	D0
13	D2		14	D3		15	D2
16	D4		17	D5		18	D4
19	D6		20	D7		21	D6
22	N.C.		23	E3		24	N.C.

Table 5-7 NMIY J6 Pinouts

5.4 C8051F020TB

This is at the time of writing, one of the latest super-charged versions of the 8051 family. It is the product of Silicon Labs.

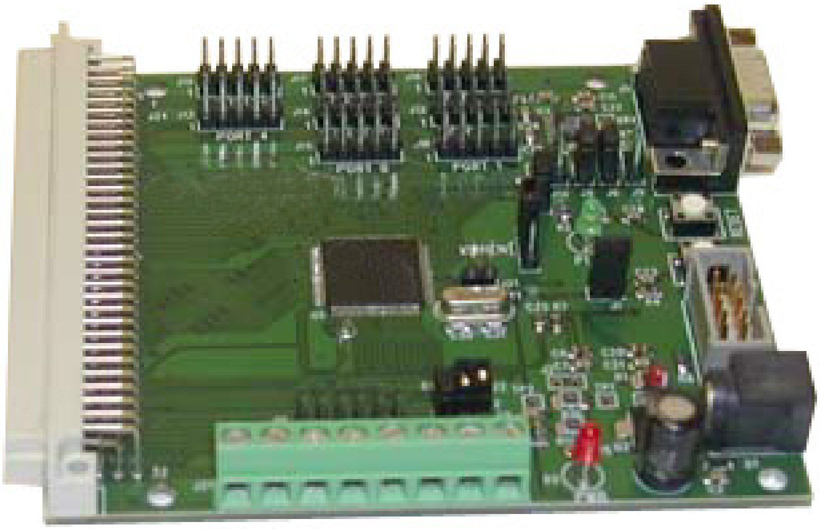

Figure 5-3 C8051F020 Board

Further details, manuals and example programs can be found at the Silicon Labs site, whose contact details are being listed here under:

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